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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mansoori et al.	Art Unit:	2812
Serial No.:	10/620,492	Examiner:	Lindsay, Jr., W.
Filing Date:	07/16/2003	Docket No.:	TI-35375
Customer No.:	23494	Conf. No.:	9069

Title: METHOD TO REDUCE TRANSISTOR GATE TO SOURCE/DRAIN OVERLAP CAPACITANCE BY INCORPORATION OF CARBON

ELECTION

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as first Class Mail in an envelope addressed to Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

9-16-04
Date
Marianna Smith
Marianna Smith

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

With respect to the Restriction Requirement mailed on 08/23/2004, the Examiner has restricted the instant application to the invention of Group I (Claims 36-44), or Group II (Claims 1-35). In light of this, Applicants elect to pursue Group II, (Claims 1-35) and species I (Claims 1-28) without traverse.

Respectfully submitted,

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